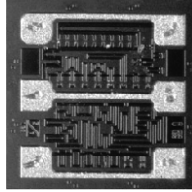


Dual Resistor Divider Thin Film Custom Network



Product may not be to scale

FEATURES

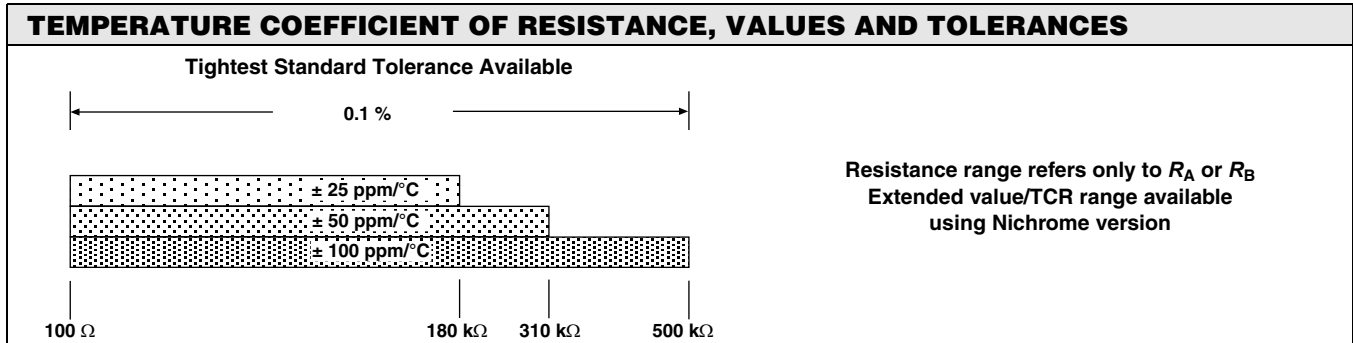
- Wire bondable
- Individual value and tolerance selection
- Ratio tolerance to 0.05 %
- Chip size: 0.030 inches square
- Resistance range: 100 Ω to 500 kΩ
- Oxidized silicon substrate for good power dissipation
- Resistor material: Tantalum nitride, self-passivating

The STR, DTR series of dual resistor dividers provides the user with the option to specify the value, tolerance of each individual resistor and ratio tolerance.

The dual resistor dividers are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The dual resistor dividers are 100 % electrically tested and visually inspected to MIL-STD-883.

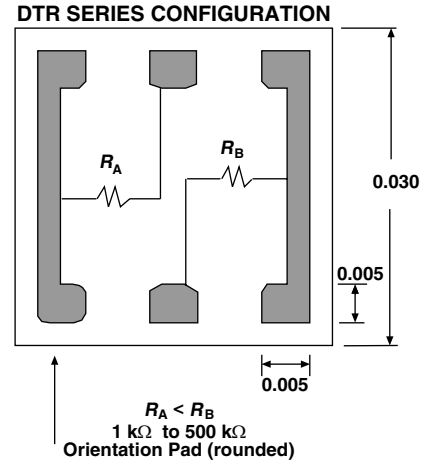
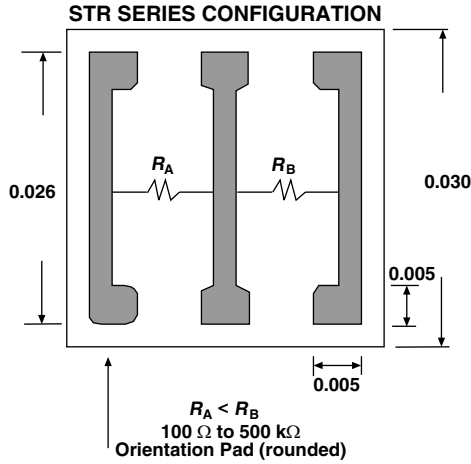
APPLICATIONS

Vishay EFI custom-made two resistor chips are designed for hybrid packages requiring close ratio-matching and tracking of two different resistors for gain accuracy and stability. The customized resistance values give the hybrid designer greater flexibility.



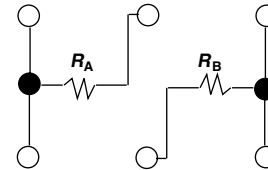
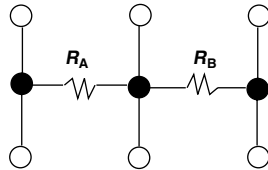
STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
TCR Tracking Between Halves (R_A/R_B)	± 10 ppm/°C, ($R_A < 1K$) ± 5 ppm/°C, ($R_A ≥ 1K$)
Resistance Ratio Tolerance R_A/R_B	Customer specified to 0.05 %
Noise, MIL-STD-202, Method 308 100 Ω - 250 kΩ < 100 Ω or > 251 kΩ	- 35 dB typ. - 20 dB typ.
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 % max. $\Delta R/R$
Stability, 1000 h, + 125 °C Derated Power	± 0.2 % max. absolute ± 0.02 max. ratio
Operating Temperature Range	- 55 °C to + 125 °C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.1 % max. $\Delta R/R$
High Temperature Exposure, + 150 °C, 100 h	± 0.2 % max. $\Delta R/R$
Dielectric Voltage Breakdown	200 V
Insulation Resistance	10 ¹² min.
Operating Voltage	100 V
DC Power Rating at + 70 °C (Derated to Zero at 175 °C)	125 mW each resistor
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.1 % max. $\Delta R/R$

DIMENSIONS in inches



CHIP RESISTORS

SCHEMATIC



MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip Size	0.030 x 0.030 ± 0.003 (0.762 x 0.762 ± 0.05 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO ₂
Resistor Material	Tantalum nitride, self-passivating
Bonding Pad Size	0.005 x 0.005 (0.127 x 0.127 mm) minimum
Number of Pads	6
Pad Material	10 kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

Options: Gold back for eutectic die attach
Gold bonding pads, 15 kÅ minimum;
Contact Applications Engineer

ORDERING INFORMATION										
Example: 100 % visual, STR format, 1 k Ω /20 k Ω , 1 % tolerance, 0.1 % ratio, 50 ppm/ $^{\circ}$ C, aluminum pads, class H visual inspection										
W	STR	1000	0	/	2000 1	F	B	D	H	A
INSPECTION/ PACKAGING	PRODUCT FAMILY	RESISTANCE VALUE (R ₁)	MULTIPLIER CODE		RESISTANCE VALUE + MULTIPLIER (R ₂)	TOLERANCE CODE	RATIO TOLERANCE	TCR	CLASS	BOND PADS
W = 100 % visually inspected parts per MIL-STD-883 X = Sample, visually inspected loaded in matrix trays (4 % AQL)		Use first 4 digits	B = 0.01 A = 0.1 0 = 1 1 = 10 2 = 100 3 = 1000			B = 0.01 % C = 0.2 % D = 0.5 % F = 1.0 % G = 2.0 % H = 2.5 % J = 5.0 % K = 10 % K = 10 % *Coating standard	D = 0.05 % F = 0.1 % G = 0.2 % J = 0.5 % K = 1 % M = 2 % *Coating standard	B = ± 25 D = ± 50 E = ± 100 G = ± 200 standard	Class H Class K	Aluminum gold



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All product specifications and data are subject to change without notice.

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